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10/582,190	03/21/2007	Mitsuhiro Ayaki	SHIGA3.010APC	1681

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EXAMINER
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O HERN, BRENT T

ART UNIT	PAPER NUMBER
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1794

NOTIFICATION DATE	DELIVERY MODE
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07/08/2009

ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

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jcartee@kmob.com  
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## **DETAILED ACTION**

### ***Claims***

1. Claims 1, 4 and 6-10 are pending.

## **WITHDRAWN REJECTIONS**

2. All rejections of record in the Office Action mailed 11/12/2008 have been withdrawn due to Applicant's amendments in the Paper filed 4/10/2009.

## **NEW REJECTIONS**

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office Action.

### ***Claim Rejections - 35 USC § 112***

3. Claims 1, 4 and 6-10 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
4. The phrase "all of the AC chip is inserted in the penetrating openings" in claim 1, line 5 is vague and indefinite since it is unclear whether each chip is inserted in just one opening or more than one opening. FIG-3 illustrates a plurality of chips with each chip inserted in a single opening.

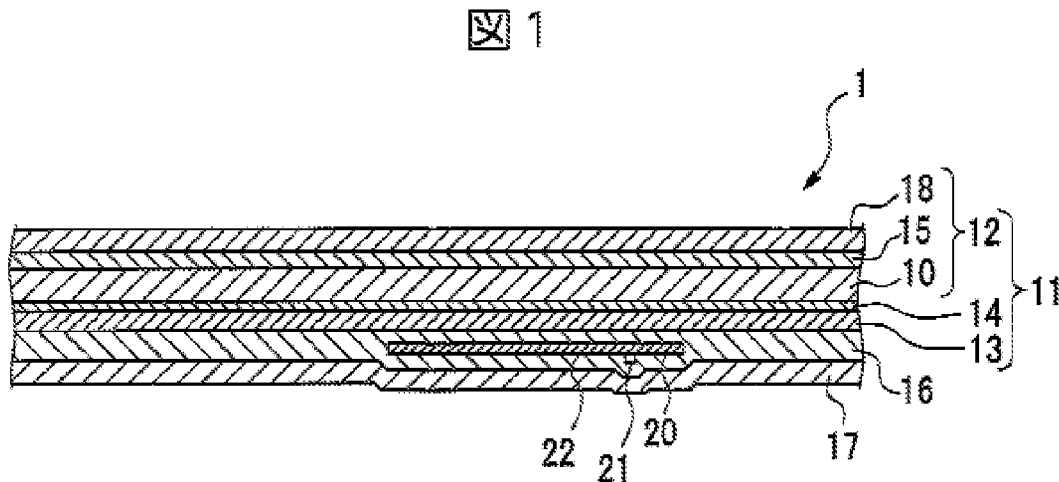
Clarification and/or correction required.

### ***Claim Rejections - 35 USC § 103***

5. Claims 1, 4 and 6-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiki et al. (WO 03/027950) with evidence by Fujiki et al. (US 2004/0262404) which is interpreted as the English language equivalent of Fujiki et al. (WO 03/027950).

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Fujiki ('950) teaches a multilayer tape/sheet with a built-in IC chip used for a sheet comprising a tape body comprising a first base material and second base material (See FIGs 1-4 and paras. 24-26, 56-58 and 97 where embedded element #20 can be an IC module #30 with IC chip #27 embedded within the multilayer tape/film #1 which is formable into a baggage tag #10 containing paper #12, resin adhesive #16, plastic resin film #13 and plastic resin protection sheet #17 and the laminate/tape being exposed at the outer surfaces/sides.),



wherein the second base material has a penetrating opening with all of the IC chip being embedded in the tape body in a non-exposed state (See FIGs 1, 3 and paras. 24-26, non-exposed element #20 that can be an IC module #30 with IC chip #27.), with the IC chip being fixed to the tape body by a resin (See FIGs 1, 3 and paras. 24-26, resin adhesive #16.), which is inserted into the sheet-like material wherein a groove is formed on the sheet-like material, and the tape is attached to the groove (See FIG 1 and paras. 24-26, where the embedded chip forms a groove within the polymeric material. The number and shapes of the grooves depending on the surface configuration of the chip.).

However, fails to expressly disclose the base material having a plurality of openings.

The configuration of the chip creates the opening which become closed when the chip embeds. Additionally, it would have been obvious to provide two or more smaller openings or one larger opening to embed the IC chip based on the configuration of the chip with the end product either being the same or substantially the same with an IC chip being embedded in the base material.

### **ANSWERS TO APPLICANT'S ARGUMENTS**

6. In response to Applicant's arguments (*pp. 4-5 of Applicant's Paper filed 4/10/2009*) regarding the new penetrating openings limitations, it is noted that said new limitations are discussed above.

7. In response to Applicant's arguments (*p. 5, para. 1 of Applicant's Paper filed 4/10/2009*) that Fujiki ('950) teaches away from the amended claims having the newly presented penetrating openings limitations because the amended claims now require the IC chip to be inserted into the penetrating openings in a non-exposed state and Fujiki ('950) does not teach penetrating openings but rather adhesive surrounding a chip, it is noted as discussed above that the configuration of the chip creates the opening which become closed when the chip embeds. Thus, the opening is closed which is also the case for Applicant's product once the chip becomes embedded. Additionally, it would have been obvious to provide two or more smaller openings or one larger opening to embed the IC chip based on the configuration of the chip with the end

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product either being the same or substantially the same with an IC chip being embedded in the base material.

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brent T. O'Hern whose telephone number is (571)272-0496. The examiner can normally be reached on Monday-Thursday, 9:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Sample can be reached on (571) 272-1376. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/BTO/  
Brent T. O'Hern  
Examiner  
Art Unit 1794  
June 24, 2009

/Elizabeth M. Cole/  
Primary Examiner, Art Unit 1794